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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,965	07/08/2003	Janko Boehm	DE920010007US1	8863

7590 05/06/2005

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,965	BOEHM ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because:

-Fig. 2 and Fig. 3 contain numerical labels without associated textual labels.

-Fig. 1 contains misspelling of the word "successful".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-57 are rejected under 35 USC 103(a) as being unpatentable over US Pat. No. 6,181,159 to Rangasayee.

4. As per claims 1, 22 and 43, Rangasayee discloses a method, computer system and program product for controlling a plurality of I/O devices (Fig. 11, elements 514 and 516 being multiple I/O ports to be attached to devices attached to them, e.g., I/O devices, Column 12, lines 28-36) being attached to a microprocessor by (Column 9, lines 5-12, microprocessor can program the programmable device, e.g., element 500 of Fig. 11) by a special number and type of interfaces (the chip is clearly attached/interfaces an external microprocessor by a special bus to connect the microprocessor; communication must be performed over a physical, electrical conduit, using a communication protocol enabling communication between the two devices) comprising: connecting a configurable chip (Fig. 11, element 500 can be an FPGA or CPLD, Column 1, lines 39-52) to the I/O space of said microprocessor (virtual circuit created programmed by the microprocessor, Column 9, lines 5-13, is accomplished through the I/O pins of the microprocessor, hence through the I/O space of the processor), said configurable chip having a switch matrix (Fig. 2-4, cross bar switch matrix); and assigning to said switch matrix said special number and type of interfaces to each I/O device (programming the switch matrix entails creating or destroying certain circuits to eventually create the desired route from I/O device to I/O device).

Rangasayee does not disclose expressly the I/O devices are initialized or the step of performing the assignments of the special number and type of interfaces during initialization.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to initialize the programmable switch matrix device such that the special routing pathways to connect the various I/O devices are established before communication begins.

The suggestion/motivation for doing so would have been programmable devices, in particularly CPLDs and FPGAs require initial instruction on how to configure the logic blocks and programmable routes on the device prior to ordinary use. This step is always done during initialization where an external source sends configuration data to the programmable device in order to configure the device for the desired functionality as is well known to one of ordinary skill in the art.

Therefore, it would have been obvious to initialize the programmable logic device according to the specification of the I/O devices, e.g., the desired routing configuration, prior to actual use.

5. As per claims 2-5 and 23-26, Rangasayee discloses claims 1 and 22, wherein the chip serves as a active element (e.g., capable of being programmed over and over, e.g., FPGA) and controls the routing of particular signals from one pin to another, and therefore by definition, being a controller. In addition, it is completely within the scope of Rangasayee where the chip is programmed merely once (or has only one configuration data) and thereby is passive acting as an ASIC.

6. As per claims 6-7, 27-28 and 44-45, Rangasayee discloses claims 1, 22 and 43 wherein the I/O devices attached to the configurable chip have various different communication protocols, Rangasayee specifically cites network applications, which intrinsically require a set of communication protocols such as TCP/IP, but also the attachment of the chip to the

microprocessor would entail usage of well known chip to chip protocols such as Hypertransport, RapidIO or I2C.

7. As per claims 8-21, 29-42 and 46-57, Rangasayee discloses claims 1,22 and 43 wherein switch matrix is configurable to the needs of the various devices attached to it (Fig. 11 shows routing is performed based on which device needs to communicate with another device), the configuration data generated by the microprocessor (Column 9, lines 1-12) or prom (FPGAS initialized generally with PROM data) dictating which virtual circuit to create.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to programmable/configurable chips for dynamically rerouting pins:

U.S. Pat. No. US005424589A to Dobbelaere et al.

U.S. Pat. No. US005646544A to Iadanza

U.S. Pat. No. US005760607A to Leeds et al.

U.S. Pat. No. US006539418B2 to Schneider et al.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
4/25/2005

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
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